

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method for a link layer protocol comprising: reserving a single buffer of a plurality of buffers for each of a plurality of virtual channels (VCs);

storing a plurality of buffer indexes corresponding to a plurality of buffers not reserved for each VC; and

sharing the buffers not reserved for each VC among a plurality of VCs.

2. (Previously Presented) The method of claim 1 wherein storing the plurality of buffer indexes comprises storing the plurality of buffer indexes in a first in first out memory (FIFO).

3. (Currently Amended) The method of claim 2 wherein the sharing the remaining buffers is based at least in part on whether the buffer is used for receiving or transmitting data.

4. (Currently Amended) The method of claim 1 wherein sharing the remaining link buffers allows for switching from one list of link units for a first VC [[is]] when blocked, the link layer by switching from the first VC's link buffer to the second

VC's link buffer.

5. (Previously Presented) An apparatus comprising:
 - a main transmit buffer and a main receiver buffer for each virtual channel (VC) for a link layer protocol of the point to point network;
 - a plurality of link buffers to be shared based at least in part on a link buffer list for each virtual channel; and
 - the main receiver and transmit buffers to be sized based at least in part on a round trip delay time.

6. (Currently Amended) The apparatus of claim 5 wherein the apparatus is a link layer component of an electronic system.

7. (Original) The apparatus of claim 5 wherein the apparatus facilitates the switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.

8. (Currently Amended) A link layer apparatus comprising:
 - a main transmit buffer and a main receiver buffer for each virtual channel (VC);
 - a main transmit buffer and a main receiver buffer for each virtual channel (VC) of the point to point network;
 - a sender component of a link unit coupled to send packets corresponding to a VC

to indicate whether the link unit utilized a reserved credit or a shared VC buffer, the reserved credit to be utilized for another a predetermined function if the shared VC buffer is used instead of the reserved credit.

9. (Canceled)

10. (Previously Presented) The link layer apparatus of claim 8 wherein the sender component facilitates a switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.

11. (Canceled)

12. (Currently Amended) A system comprising:
at least two processors coupled into a point to point network;
a main transmit buffer and a main receiver buffer for each virtual channel (VC)
of the point to point network;
a plurality of link buffers to be shared between the main transmit buffer and the main receiver buffer based at least in part on a link buffer for each virtual channel; and
a sender component of a link unit coupled to send packets corresponding to a VC
to indicate whether the link unit utilized a reserved credit or a shared VC buffer, the reserved credit be utilized for another a predetermined function if the shared VC buffer is used instead of the reserved credit.

13. (Canceled)

14. (Previously Presented) The system of claim 12 wherein the sender component facilitates a switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.

15. (Canceled)

16. (Previously Presented) A system comprising:
at least two processors coupled into a point to point network;
a main transmit buffer and a main receiver buffer for each virtual channel (VC)
for a link layer protocol of the point to point network;
a plurality of link buffers to be shared based at least in part on a link buffer list for each virtual channel; and
the main receiver and transmit buffers to be sized based at least in part on a round trip delay time.

17. (Original) The system of claim 16 wherein the link layer protocol facilitates the switch from a first VC's link buffer or FIFO to a second VC's link buffer or FIFO if the first VC's link buffer or FIFO is blocked.